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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/378,519	08/20/1999	FUMIAKI INAGE	9281-3394	9240

757 7590 12/28/2004

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EXAMINER	
ANYASO, UCHENDU O	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/378,519	INAGE, FUMIAKI	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1** and **3-11** are pending in this action.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1** and **3-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Fuse* (U.S. Patent 4,642,693) in view of Yamagishi (U.S. 4,642,694).

Regarding **claims 1** and **6**, Fuse teaches an invention relating to an improvement in a television video signal A/D converter apparatus for a liquid crystal television receiver (column 1, lines 5-9).

Furthermore, Fuse teaches a plurality of A/D converters (33-35) that convert a luminance signal as represented by the RGB color signals from the color television video signal (column 4, lines 12-41, figure 4 at 33-35).

Furthermore, Fuse teaches a plurality of setting circuits by teaching reference potential generators (36-38) which facilitate the generation of upper and lower reference potentials VH and VL that are supplied to the A/D converters (33-35) (column 4, lines 16-21, figure 4 at 33-38).

Also, Fuse teaches a variable power supply connected to one of the A/D converters (33) by teaching power supply in combination with a variable resistor to generate VH and VL wherein the VH defines a maximum value of the input signal to the A/D converter (33) such that the power supply in combination with a variable resistor controls how the upper and lower reference potentials are changed, thus adjusting contrast (column 3, lines 59 through column 4, line 2).

Furthermore, Fuse teaches a second power source Vcc that is connected to A/D converter (34) that also general a lower voltage limit VL corresponding to a minimum value of the of the digital signal DG1-DG4 that is outputted from one of the converters (column 4, lines 16-25).

Also, Fuse teaches how to achieve a plurality of intermediate voltage circuits that sets intermediate voltages between the upper limit voltages and the lower limit voltages by teaching how the average value is fixed to a DC voltage level at the node B, i.e., a constant potential determined by the resistors 22, 23, 24 and 25, as shown in FIG. 3(b) such that in order to reduce influence of the vertical and horizontal synchronizing signals, the average value is preferably set at a value which is shifted from an intermediate value between the DC potentials at the nodes C and D to the node D side by dividing the DC potential at the node B (column 3, lines 53-59, figures 2, 3a-3c).

However, Fuse does not teach how a plurality of setting circuits that sets magnitudes of reference voltage ranges to determine upper and lower limit voltages of the digital signals would be identical in each of the converters. On the other hand, Yamagishi teaches how such a concept would be accomplished manually by teaching a plurality level shifters (setting circuits) that sets the levels/magnitudes of the VH' and VL' signals in each of the converters wherein the

respective levels of VH' and VL' in each of the A/D converters 41a-41c have the capability of being manually adjusted in the level shifters 47a-47c via 6a1-6bc1 respectively (figure 12 at 41a-41c, 47a-47c & 6a1-6bc1).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Fuse and Yamagishi because while Fuse teaches how a variable power supply would be connected to the A/D converters such that the power supply in combination with a variable resistor controls how the upper and lower reference potentials are changed, thus adjusting contrast (column 3, lines 59 through column 4, line 2), Yamagishi teaches how to manually achieve identical VH and VL levels in each of the A/D converters by means of a plurality level shifters (setting circuits) that sets the levels/magnitudes of the VH' and VL' signals in each of the converters wherein the respective levels of VH' and VL' in each of the A/D converters 41a-41c have the capability of being manually adjusted in the level shifters 47a-47c via 6a1-6bc1 respectively (figure 12 at 41a-41c, 47a-47c & 6a1-6bc1). The motivation for doing so would have been to achieve excellent image contrast and clear gradations near the black and white levels (column 2, lines 5-12).

Regarding **claims 3** and **8**, in further discussion of claims 1 and 6, Fuse teaches a second power that is a fixed power supply by teaching Vcc, VH and VL (figure 4 at 37).

Regarding **claims 4** and **7**, in further discussion of claims 1 and 6, Fuse teaches a variable power supply connected to one of the A/D converters (33) by teaching power supply in combination with a variable resistor to generate VH and VL wherein the VH defines a maximum

value of the input signal to the A/D converter (33) such that the power supply in combination with a variable resistor controls how the upper and lower reference potentials are changed, thus adjusting contrast (column 3, lines 59 through column 4, line 2).

Furthermore, Fuse teaches a second power source Vcc that is connected to A/D converter (34) that also general a lower voltage limit VL corresponding to a minimum value of the of the digital signal DG1-DG4 that is outputted from one of the converters (column 4, lines 16-25).

Regarding **claims 5** and **9**, in further discussion of claim 1, Fuse teaches how the amplitudes of the color signals can be adjusted to proper levels by adjusting the contrast such that the controls of the generators 36 and 38 for R and B signals are adjusted so as to change reference levels of the R and B signals for A/D conversion without changing a reference level of the G signal therefrom so as to change levels of the digital signals DR1 to DR4 and DB1 to DB4, thus displaying proper colors on the liquid crystal panel (column 4, lines 30-38, figure 4).

Regarding **claims 10** and **11**, Yamagishi teaches how the intermediate voltage values correspond to a white level and a black level in each of the two color difference signals (column 8, lines 67 through column 9, lines 35).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi, can be reached at (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

12/23/2004

CHANH NGUYEN
PRIMARY EXAMINER